Docket No: G0615

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re **PATENT** application of:

Applicant:	Bin Yu, et al.
Application No.:	10/044,493
Filing Date:	January 11, 2002
Title:	SEMICONDUCTOR DEVICE WITH SILICIDE SOURCE/DRAIN AND HIGH-K DIELECTRIC
Examiner:	Kevin V. Quinto
Art Unit:	2826

Confirmation No.: 9266

APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This brief is being submitted in connection with the appeal of the above-identified application.

I. Real Party in Interest

The real party in interest in the present appeal is Advanced Micro Devices, Inc., the assignee of the present application.

II. Related Appeals and Interferences

Appellant, appellant's undersigned representative, and/or the assignee of the present application are unaware of any appeals or interferences which will directly affect, which will be directly affected by, or which will have a bearing on the Board's decision in the pending appeal.

III. Status of Claims

Claims 1-10 and 20 are pending in the application, stand finally rejected and are the subject of this appeal. A correct copy of claims 1-10 and 20 appears in Appendix A attached hereto.

IV. Status of Amendments

A Response filed on January 16, 2003 to the final Office Action mailed December 4, 2002 contained an amendment placing dependent claim 20 in independent form. In an Advisory Action dated February 14, 2003, the Examiner indicated that the amendment would not be entered for purposes of appeal. A Supplemental Reply to the final Office Action mailed December 4, 2002 was filed on February 26, 2003. The Examiner indicated that the amendment contained within the Supplemental Reply would not be entered for purposes of appeal.

V. Summary of Invention

A pervasive trend in integrated circuit manufacture is to produce semiconductor devices, such as metal oxide semiconductor field effect transistors (MOSFETs), that are as small as possible. While the fabrication of smaller transistors allows more transistors to be placed on a single monolithic substrate for the formation of relatively large circuit systems in a relatively small die area, this downscaling can result in a number of performance degrading effects. For example, a problem in the prior art has been that certain materials selected to be used in a downscaled device may react with other

materials and/or become degraded when a thermal budget for the materials is exceeded (for example and depending on the material, when an anneal cycle approaches about 1000°C).[1]

Conventional semiconductor devices (e.g., the devices disclosed in Wilting[2] and Grant[3]) include source and drain regions formed with conventional ion implantation. Ion implantation is usually followed by one or more associated anneal cycles to activate those dopant species and/or recrystalize the layer of semiconductor material.

These additional anneal cycles, as well as other thermal cycles used to fabricate the prior art devices, can adversely affect the structural features and integrity of the device. For example, the additional thermal processing associated with the conventional devices may exceed the thermal budget of one or more materials in the device, such as the gate dielectric material, which could lead to the material becoming unstable, the material losing its electrical characteristics, and/or an undesirable reaction with other materials in the device.

In particular, high-K dielectric materials (i.e., as defined in the specification, materials having a relative permittivity of greater than 10 or greater than 20)[4] are often sensitive to excessive thermal processing.

The present invention recognizes that a problem exists with respect to the instability of high-K materials when a thermal budget for the high-K material is exceeded (e.g., due to anneal cycles associated with ion implantation to activate dopant species and/or recrystalize the implanted semiconductor material). Further, the present invention provides a solution to this problem that is neither contemplated, disclosed nor otherwise suggested by the prior art.

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[1] See specification, page 1, lines 20-23.

[2] U.S. Patent No. 4,080,719.

[3] U.S. Patent No. 6,423,619.

[4] See specification, page 4, lines 18-24.

The present invention addresses this problem by providing a semiconductor device including a source and a drain, which consist essentially of silicide, and a gate dielectric made from a high-K material (i.e., a dielectric material having a relative permittivity greater than 10).[5] The silicide source and drain are formed by reacting a metal layer 74 with a layer of semiconductor material 18 such that the source and drain are formed without the use of conventional ion implantation. Forming a semiconductor device, having a silicide source and drain and a high-K gate dielectric, without conventional ion implantation, provides a device with improved structure and performance.

More particularly, according to one aspect of the invention, the invention is directed to a semiconductor device 10. The semiconductor device 10 includes a source 20 and a drain 22, which each consist essentially of silicide. A semiconductor body 24 is disposed between the source 20 and the drain 22. A gate electrode 28, which is disposed over the body 24, defines a channel interposed between the source 20 and the drain 22. A gate dielectric 30, made from a high-K material, separates the gate electrode and the body 24.

According to one embodiment of the invention, a source/body junction is defined by silicide material of the source 20 and semiconductor material of the body 24. In addition, a drain/body junction is defined by silicide material of the drain 22 and semiconductor material of the body 24.

In sum, the invention defined in the claims on appeal stems from the appellants' appreciation of the advantages of achieving a semiconductor device that optimizes scale and performance by including a source and a drain each consisting essentially of silicide and a gate dielectric made from a high-K material.

VI. Applied Prior Art

U.S. Patent No. 4,080,719 to Wilting;

U.S. Patent No. 6,423,619 to Grant et al.;

U.S. Pat. Application Pub. No. 2001/0031562A1 to Raajimakers et al.; and

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[5] Id.

U.S. Patent No. 5,736,435 to Venkatesan et al.

VII. Issues

A. Whether claims 1-4, 8, 9 and 20 are properly rejected under 35 U.S.C. §102(b) as being anticipated by Wilting.

B. Whether claims 1-5, 8, 9 and 20 are properly rejected under 35 U.S.C. §103(a) as being unpatentable over Grant et al. in view of Wilting.

C. Whether claims 6 and 7 are properly rejected under 35 U.S.C. §103(a) as being unpatentable over Grant et al. in view of Wilting and further in view of Raajimakers.

D. Whether claim 10 is properly rejected under 35 U.S.C. §103(a) as being unpatentable over Wilting in view of Venkatesan et al.

E. Whether claim 10 is properly rejected under 35 U.S.C. §103(a) as being unpatentable over Grant et al. in view of Wilting and further in view of Venkatesan.

VIII. Grouping of Claims[6]

For the purposes of this appeal only, the claims are grouped as follows:

Claims 1-10 stand or fall together. Claim 20 stands separately for the reasons articulated herein below.

IX. Argument

Claims 1-4, 8 and 9 have been finally rejected as being anticipated by Wilting. The Examiner contends:

> Wilting (USPN 4,080,719) discloses a similar device. Figure 16 illustrates a MOSFET with a source (31) and a drain (32).

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[6] This grouping is conditioned upon the Examiner not entering any new grounds of rejection and/or any new points of argument.

> Wilting discloses that the source and drain regions (31, 32) are entirely silicide (column 7, lines 46-47); thus meeting and exceeding the "essentially of silicide" limitation. . . . There is a gate dielectric (4A, 4B), made of silicon oxide (4A) and silicon nitride (4B), which separates the gate electrode (16A) and the body. The silicon oxide - silicon nitride is a well-known high-K or high dielectric film (see Lee, USPN 5,693,554, column 5, lines 30-31).[7]

It is respectfully submitted that the Examiner has failed to establish that claim 1 is anticipated by Wilting. Further, it is respectfully submitted that the Examiner fails to appreciate the meaning of at least one of the claim limitations. As such, the Examiner has also failed to establish a *prima facie* case of obviousness with respect to the additional rejections discussed below.

At the outset, Appellant notes that under 35 U.S.C. §102, "[a] claim is anticipated only if each and every element of the claim is found, either expressly or inherently described, in a single prior art reference."[8] In short, it is respectfully submitted that the Examiner has failed to establish that claim 1 is anticipated by Wilting because Wilting fails to disclose or fairly suggest all of the claim limitations.

Turning to claim 1, a semiconductor device is claimed. Claim 1 calls for, *inter alia*, a source and a drain, where the source and the drain **consist essentially of silicide**, and a gate dielectric made from **a high-K material**, that is, **a gate dielectric having a K of greater than 10, in one embodiment, and greater than 20** in another embodiment.[9]

With regard to the term, "high-K material", appellant notes that, "when the specification states the meaning that a term in the claim is intended to have, the claim is

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[7] Final Rejection (12/04/02), paragraph 5.

[8] MPEP §2131, *citing*, *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

[9] See specification, page 4, lines 18-24.

examined using that meaning, in order to achieve a complete exploration of the applicant's invention and its relation to the prior art."[10]

As such, Wilting fails to disclose or fairly suggest a semiconductor device, which includes a high-K gate dielectric. In contrast to the assertion at paragraph 5 of the Office Action, neither silicon oxide nor silicon nitride, standing alone as a single layer or formed together as stacked layers, constitute a high-K gate dielectric, as defined by the applicant. In particular, silicon oxide has a K of approximately 3.9 (see, for example, page 5, lines 16-17 of the present application and Grant at col. 1, line 15), while silicon nitride has a K of approximately 6-9 (see, for example, page 5, lines 6-7 of the present application).

Further, the Office Action's reliance on Lee[11] for a showing that silicon oxide and silicon nitride (as used and disclosed by Wilting) are high-K materials is inappropriate. First, at col. 5, lines 30-31, Lee does not discuss silicon oxide or silicon nitride. Rather, Lee discusses a "NO (Nitride-Oxide)" layer, which is not a conventional chemical expression and, at best, can be interpreted as silicon oxynitride, having a K of about 4-8. Second, even if Lee referred to one or both of silicon nitride and silicon oxide as "high-K materials," this characterization is irrelevant in light of appellants' clear enumeration of the meaning of the claim term within the specification of the application.

The Examiner's apparent lack of appreciation of the meaning of the term "high-K dielectric" is also apparent in light of the reference made to Topich[12] in the Examiner's Advisory Action of February 14, 2003. In this Action, the Examiner contends:

> [t]he arguments presented appear to be dependent upon the statement that an oxide nitride stack is not considered to have a high dielectric constant. However the examiner would like to point out that Topich (USPN 4,419,812),

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[10] MPEP §2173.05(a), *citing*, *In re Zletz*, 893 F.2d 319, 13 USPQ2d 1320 (Fed. Cir. 1989).

[11] U.S. Patent No. 5,693,554.

[12] U.S. Patent No. 4,419,812.

which uses an oxide nitride stack and describes it as having a high dielectric constant (column 8, lines 34-38).

As discussed above, Topich's characterization of an oxide nitride stack is irrelevant in light of appellants' clear enumeration of the meaning of the claim term within the specification of the application.

In addition, Wilting fails to disclose or fairly suggest a semiconductor device, which includes a source and a drain consisting essentially of silicide. Paragraph 5 of the Office action points to col. 7, lines 46-47 of Wilting, alleging that Wilting "discloses that the source and drain regions (31, 32) are entirely silicide." However, appellants respectfully submit that this language is taken out of context. In particular, the description found at col. 7, lines 46-55 of Wilting describes **Figure 16, which illustrates silicide drain zones (31) and (32) within p-type drain zones (41) and (42) (designated by dashed lines in Figures 14-16)**.

More particularly, Figures 14-16 of Wilting, along with the associated description in column 7, clearly differentiate between the source and drain zones (41) and (42) and source and source and drain zones (31) and (32). P-type source and drain zones (41) and (42) are formed by "indiffusion or implantation." (see, for example, col. 7, lines 49-50). For these reasons alone, claim 1 is neither anticipated nor rendered obvious by Wilting.

Not only does Wilting fail to anticipate the claimed invention, but it, taken alone or in combination with the other cited references, fails to render the claimed invention obvious.

With regard to the second rejection, claims 1-5, 8 and 9 have been finally rejected as being obvious over Grant in view of Wilting. It is respectfully submitted that the Examiner has failed to establish a *prima facie* case of obviousness.

Under 35 U.S.C. §103(a), "[t]o establish a *prima facie* case of obviousness three basic criteria must be met. First, there must be some suggestion or motivation either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be

a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations."[13]

As is discussed more fully above, Wilting fails to disclose or fairly suggest a semiconductor device, which includes a source and a drain consisting essentially of silicide. Again, Figure 16 of Wilting illustrates silicide drain zones (31) and (32) within p-type drain zones (41) and (42) (designated by dashed lines in Figures 14-16), rather than source and drain regions consisting essentially of silicide. In addition, Grant makes no mention of silcide source and drain regions.

In addition to the deficiencies of Wilting discussed more fully above, both Grant (see, for example, col. 2, lines 41-44) and Wilting (see above discussion) teach sources and drains formed using conventional ion implantation. This ion implantation must be coupled with relatively high temperature processing (e.g., about 1000°C, as disclosed in Wilting), which is prone to damage an associated high-K gate dielectric layer.

In contrast, the present invention discovered the source of a problem involving the thermal budget of high-K gate dielectric materials and provided a solution (i.e., a device having a silicide source and drain formed without ion implantation).

In this regard, it is noted that "a patentable invention may lie in the discovery of the source of a problem even though the remedy may be obvious once the source of the problem is identified."[14] Appellants acknowledge that those who allege discovery of the source of a problem and solution must provide substantiating evidence. MPEP 2141.02.

In this case, appellant, at the time of the invention, discovered that a need exists for a semiconductor device having a stable, quality high-K dielectric layer that is not compromised (i.e., the thermal budget is not exceeded, causing the material becoming unstable, to lose its electrical characteristics, and/or to react undesirably with other

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[13] MPEP §2142, *citing*, *In re Vaeck*, 947F.2d. 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

[14] MPEP 2141.02, *citing, In re Sponnoble*, 160 U.S.P.Q. 237, 243 (CCPA 1969).

materials in the device) due to thermal processing associated with anneal cycles following source and drain ion implantation.

Evidence of the discovery of the source or cause of this problem, i.e., instability of high-K materials when a thermal budget for the high-K material is exceeded (e.g., following anneal cycles to activate dopant species forming the source and/or drain), can be found in Appellant's Patent Application at page 10, lines 17-29.

Further, in response to the discovered problem, appellant developed a solution to the problem. A semiconductor device was created that includes a quality high-K dielectric layer, which is not compromised by additional thermal processing required by high temperature anneal cycles following ion implantation. Rather, a device having a source and a drain consisting essentially of silicide is formed with low temperature processing (e.g., about 350°C to about 450°C) and without conventional ion implantation. These limitations, which solve the discovered problem, are present in claim 1 and distinguish the invention patentably over the references of record.

Accordingly, the rejections of claim 1 and the claims depending therefrom, including claims 2-10 and 20, should be removed.

Claim 20 has been finally rejected as being anticipated by Wilting and, alternatively, as being obvious over Grant in view of Wilting.

For at least the reasons discussed above, the rejection of claim 20 as being anticipated by Wilting should be removed. In addition, with respect to the alternative rejection of claim 20, it is respectfully submitted that neither Grant nor Wilting, taken alone or in combination with each other and/or any of the other cited references, disclose or fairly suggest the claimed invention.

Regarding dependent claim 20, claim 20 recites that "**a source/body junction is defined by silicide material of the source and semiconductor material of the body and a drain/body junction is defined by silicide material of the drain and semiconductor material of the body**." (Emphasis added).

None of the cited references, taken alone or in combination, disclose or fairly suggest source/body and drain/body junctions defined by silicide material of the source/drain and semiconductor material of the body.

In this regard, appellant respectfully submits that what is alleged in paragraphs 9 and 16 of the Office action is simply inaccurate. In particular, both of paragraphs 9 and 16 of the Office action point to Figure 16 of Wilting for the teaching of source/body and drain/body junctions defined by silicide material of the source/drain and semiconductor material of the body. However, **Figure 16 of Wilting, along with the associated description at column 7, clearly shows silicide source zone (31) within implanted p-type source zone (41) (shown by dashed line) and silicide drain zone (32) within implanted p-type drain zone (42) (shown by dashed line)**. As such, the source/body junction of the device disclosed in Wilting is defined by the p-type semiconductor material of source zone (41) and the semiconductor material of the body. Similarly, the drain/body junction of the Wilting device is defined by the p-type semiconductor material of drain zone (42) and the semiconductor material of the body.

The other cited references, including Raajimakers et al. and Venkatesan et al., fail to cure the deficiencies of both Wilting and Grant.

Therefore, the rejections of claim 20 should be reversed for these additional reasons.

X. Conclusion

In view of the foregoing, the Appellant respectfully submits that the claims are patentable over the applied art and that the final rejection should be reversed.

This brief is being submitted in triplicate along with a check in the amount of $320.00 to cover the fee set forth in 37 C.F.R. § 1.17.

Should a petition for an Extension of Time be necessary for the timely reply to the outstanding Office Action (or if such petition has been made and an additional extension is necessary) petition is hereby made and the Commissioner is Authorized to charge any fees to Deposit Account No. 18-0988 Order No. G0615.

Respectfully submitted,
RENNER, OTTO, BOISSELLE & SKLAR, L.L.P.

By _____
Jason A. Worgull; Reg. No. 48,044

June 9, 2003

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CERTIFICATE OF MAILING (37 CFR 1.8a)

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June 9, 2003	Kim Hill	_____
Date	Name of person mailing paper	Signature

APPENDIX A
Claims on Appeal

1. A semiconductor device comprising:

a source and a drain, said source and drain consisting essentially of silicide;

a semiconductor body disposed between the source and the drain;

a gate electrode disposed over the body and defining a channel interposed between the source and the drain; and

a gate dielectric made from a high-K material and separating the gate electrode and the body.

2. The semiconductor device according to claim 1, wherein the semiconductor device is configured as a MOSFET.

3. The semiconductor device according to claim 1, wherein the gate is comprised of a metal containing material.

4. The semiconductor device according to claim 3, wherein the gate electrode is composed of one or more materials selected from titanium nitride, tantalum nitride, tungsten, tantalum, aluminum, nickel, ruthenium, rhodium, palladium, platinum and combinations thereof.

5. The semiconductor device according to claim 1, wherein the high-K material is composed of one or more materials selected from hafnium oxide, zirconium oxide, cerium oxide, aluminum oxide, titanium oxide, yttrium oxide, barium strontium titanate and mixtures thereof.

6. The semiconductor device according to claim 1, further comprising a buffer interface disposed between the body and the gate dielectric.

7. The semiconductor device according to claim 6, wherein the buffer interface is formed from an oxide having a thickness of about 0.5 nm to about 0.7 nm.

8. The semiconductor device according to claim 1, wherein the silicide of the source and the drain is formed by reacting nickel with a layer of semiconductor material, the body being formed from the layer of semiconductor material.

9. The semiconductor device according to claim 1, further comprising a liner disposed adjacent sidewalls defined by the gate electrode and gate dielectric.

10. The semiconductor device according to claim 1, wherein the body is formed from a semiconductor film disposed on an insulating layer, the insulting layer being disposed on a semiconductor substrate.

20. The semiconductor device according to claim 1, wherein a source/body junction is defined by silicide material of the source and semiconductor material of the body and a drain/body junction is defined by silicide material of the drain and semiconductor material of the body.

* * *